UNITED STATES PATENT AND TRADEMARK OFFICE

A

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/668,136	09/22/2003	Kirt Reed Williams	10010900-1	2011

7590 02/24/2006

AGILENT TECHNOLOGIES, INC.
Intellectual Property Administration
Legal Department, DL429
P.O. Box 7599
Loveland, CO 80537-0599

EXAMINER	
PAREKH, NITIN	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 02/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/668,136	WILLIAMS, KIRT REED	
	Examiner	Art Unit	
	Nitin Parekh	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09-22-03* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. In view of the appeal brief filed on 12-08-05, PROSECUTION IS HEREBY REOPENED.

A. A new ground of rejection for the claims 1-15 is set forth below.

2. To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Wojnarowski (US Pat. 5888884).

Regarding claim 1, Wojnarowski discloses a semiconductor structure (Fig. 8) comprising:

- a semiconductor core/die (70 in Fig. 8) having a major/top horizontal surface and half-barrel shaped side surfaces (see left/right vertical surfaces within holes 50 in Fig. 8 and Fig. 5-7; Col. 7, lines 1-10) including a first/left and a second/right half-barrel shaped side surface, the major surface being orthogonal to the side surfaces
- the semiconductor core/die material being a conventional silicon wafer/single crystal silicon (Col. 1-6)
- a continuous layer of insulating material on the half-barrel shaped side surfaces (see 54 on top, bottom and half-barrel shaped side surfaces in Fig. 3-8; Col. 7, lines 15-18), the insulating material including oxides of silicon such as SiO or SiO2 (Col. 7, lines 16-28)
- a plurality of interconnects/pads being positioned (see 40 in Fig. 8) over the major surface of the semiconductor core/die, the plurality of pads being on left/right sides to provide the desired high density interconnect (HDI) structure (see Col. 6, lines 39-45)
- a plurality of electrically isolated and patterned electrodes/channels arrayed along the continuous layer of the insulating material on the half-barrel shaped side surfaces including each first/left and right/second sides (see one of the

plurality of 62/64, shown as being connected with respective one of the plurality of interconnects/pads 40 on each half-barrel shaped side surface in Fig. 8; Col. 6, lines 37-43; Col. 7, lines 49-65; also see Col. 7, lines 63-65) and additionally arrayed over a major surface of the semiconductor core (see 62 on a top/horizontal surface connecting those on the side surfaces in Fig. 8)

- the electrically isolated/patterned electrodes/channels including a conductive material such as aluminum, tungsten, etc. (Col. 7, line 44), such material being different than the insulating oxide material and having etch selectivity with respect to the insulating material
- the isolated/patterned electrodes extending substantially in a direction orthogonal to the major surface (see portions 62 of the electrodes/channels in Fig. 8) of the semiconductor core, and
- the plurality of interconnects/pads being positioned over the major surface of the semiconductor core/die and being electrically connected to respective/selected electrically isolated/patterned electrodes to achieve the desired power, ground or other/input-output (I/O) connections (Fig. 8; Col. 7, lines 45-65)

(Fig. 8; Col. 6, line 20- Col. 8, line 20).

Regarding claims 2-9, Wojnarowski disclose the entire structure as applied to claim 1 above.

Regarding claims 10-15, Wojnarowski disclose the entire structure as applied to claims 1-9 above.

Response to Arguments

5. A. Applicant's arguments with respect to the combination of Wojnarowski with Greywall are moot in view of the new ground(s) of rejection.

B. Applicant contends that Wojnarowski does not disclose electrically isolated electrodes along said continuous layer of insulating material on said side surface as recited in claims 1 and 10.

However, as explained in the claim rejections above, the insulating layer 54 is continuous along the top, bottom and half-barrel shaped side surfaces (see 54 on top, bottom and half-barrel shaped side surfaces in Fig. 3-8; Col. 7, lines 1-18) and the electrically isolated and patterned electrodes/channels are arrayed along the continuous layer of the insulating material on the top, bottom and half-barrel shaped side surfaces (see one of the plurality of 62/64 in Fig. 8).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 571-272-1663. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAN or Public PAG. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAG system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

N. Tin Parekh

NP

02-06-06

NITIN PAREKH
PRIMARY EXAMINER
TECHNOLOGY CENTER 2800

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800